CLAIMS

What is claimed is:

1. A pulse width modulation regulator, comprising:

a charge pump;

a comparator circuit coupled to the charge pump, the comparator circuit for providing an output voltage; and

a latch circuit coupled to the charge pump for ensuring that the charge pump is adjusted such that an undershoot condition and an overshoot condition of the output voltage is minimized.

2. The regulator of claim 1, wherein an input of the comparator circuit comprises an output of the charge pump.

3. The regulator of claim 1, wherein an input of the latch circuit comprises the output voltage.

4. The regulator of claim 3, wherein the latch circuit transmits a first signal to the charge pump when the output voltage is in a first state, wherein the first signal prevents the overshoot condition.

5. The regulator of claim 4, wherein the first signal prevents the output of the charge pump from increasing further.

6. The regulator of claim 4, wherein in the first state, the output voltage goes high during a clock cycle.

7. The regulator of claim 3, wherein the latch circuit transmits a second signal to the charge pump when the output voltage is in a second state, wherein the second signal prevents the undershoot condition.

8. The regulator of claim 7, wherein the second signal prevents the output of the charge pump from decreasing further.

9. The regulator of claim 7, wherein in the second state, the output voltage goes low during a clock cycle.

10. The regulator of claim 1, wherein the latch circuit comprises:

a first SR latch;

a second SR latch, wherein an input of the second SR latch comprises the output voltage;

a first gate, wherein an input of the first gate comprises an output from the second SR latch and an input signal, wherein an output of the first gate comprises a first signal to the charge pump, wherein the first signal prevents the overshoot condition; and

a second gate, wherein an input of the second gate comprises an output from the first SR latch and the input signal, wherein an output of the second gate comprises a second

signal to the charge pump, wherein the second signal prevents the undershoot condition.

11. The regulator of claim 10, wherein the latch circuit further comprises:

a first D flip-flop coupled between the first SR latch and the second gate; and

a second D flip-flop coupled between the second SR latch and the first gate.

12. The regulator of claim 1, wherein the comparator circuit comprises:

a clock circuit; and

an inverter coupled to an output of the clock circuit.

13. The regulator of claim 1, wherein the comparator circuit comprises:

a clock circuit; and

a pulse generator coupled to an input of the clock circuit.

14. A pulse width modulation regulator, comprising:

a charge pump;

a voltage comparator circuit, wherein an input of the voltage comparator circuit comprises an output of the charge pump; and

a latch circuit, wherein an input of the latch circuit comprises an output from the voltage comparator circuit,

wherein the latch circuit transmits a first signal to the charge pump when the output from the voltage comparator circuit is in a first state, wherein the first signal prevents

an overshoot of a desired output voltage,

wherein the latch circuit transmits a second signal to the charge pump when the output from the voltage comparator circuit is in a second state, wherein the second signal prevents an undershoot of the desired output voltage.

15. The regulator of claim 14, wherein the transmission of the first signal prevents the output of the charge pump from increasing further.

16. The regulator of claim 14, wherein the transmission of the second signal prevents the output of the charge pump from decreasing further.

17. The regulator of claim 14, wherein the latch circuit comprises:

a first SR latch;

a second SR latch, wherein an input of the second SR latch comprises the output signal from the voltage comparator circuit;

a first gate, wherein an input of the first gate comprises an output from the first SR latch and an input signal, wherein an output of the first gate comprises the second signal; and

a second gate, wherein an input of the second gate comprises an output from the second SR latch and the input signal, wherein an output of the second gate comprises the first signal.

18. The regulator of claim 17, wherein the latch circuit further comprises:

a first D flip-flop coupled between the first SR latch and the first gate; and

a second D flip-flop coupled between the second SR latch and the second gate.

19. The regulator of claim 14, wherein in the first state, the output signal from the voltage comparator circuit goes high during a clock cycle.

20. The regulator of claim 14, wherein in the second state, the output signal from the voltage comparator circuit goes low during a clock cycle.

21. The regulator of claim 14, wherein the voltage comparator circuit comprises:

a clock circuit; and

an inverter coupled to an output of the clock circuit.

22. The regulator of claim 14, wherein the voltage comparator circuit comprises:

a clock circuit; and

a pulse generator coupled to an input of the clock circuit.

23. A pulse width modulation regulator, comprising:

a charge pump;

a voltage comparator circuit, wherein an input of the voltage comparator circuit comprises an output of the charge pump; and

a latch circuit, comprising:

a first SR latch,

a second SR latch, wherein an input of the second SR latch comprises an output from the voltage comparator circuit,

a first gate, wherein an input of the first gate comprises an output from the first SR latch and an input signal, wherein the first gate transmits a first signal to the charge pump when the output from the voltage comparator circuit is in a first state, wherein the first signal prevents the output from the charge pump from increasing further, and

a second gate, wherein an input of the second gate comprises an output from the second SR latch and the input signal, wherein the second gate transmits a second signal to the charge pump when the output from the voltage comparator circuit is in a second state, wherein the second signal prevents the output from the charge pump from decreasing further.

24. The regulator of claim 23, wherein the latch circuit further comprises:

a first D flip-flop coupled between the first SR latch and the first gate; and

a second D flip-flop coupled between the second SR latch and the second gate.

25. A pulse width modulation regulator, comprising:

a first controller, wherein the first controller receives as input a clock signal and a first control signal and outputs a first pulse width modulated signal;

a second controller, wherein the second controller receives as input an inverse of the clock signal and a second control signal and outputs a second pulse width modulated signal,

wherein the first control signal maintains the second pulse width modulated signal at a first state when the first pulse width modulated signal has not increased to a desired pulse width,

wherein the second control signal maintains the first pulse width modulated signal at a second state when the second pulse width modulated signal has not decreased to the desired pulse width; and

an OR gate for receiving as input the first and second pulse width modulated signals and for providing an output signal.

26. The regulator of claim 25, wherein at least the first or the second controller comprises:

a charge pump;

a comparator circuit coupled to the charge pump, the comparator circuit for providing a pulse width modulated signal; and

a latch circuit coupled to the charge pump for ensuring that the charge pump is adjusted such that an undershoot condition and an overshoot condition of the pulse width modulated signal is minimized.

27. The regulator of claim 26, wherein an input of the comparator circuit comprises an output of the charge pump.

28. The regulator of claim 26, wherein an input of the latch circuit comprises the

pulse width modulated signal.

29. The regulator of claim 28, wherein the latch circuit transmits a first latch signal to the charge pump when the pulse width modulated signal is in a high state, wherein the first latch signal prevents the overshoot condition.

30. The regulator of claim 29, wherein the first latch signal prevents the output of the charge pump from increasing further.

31. The regulator of claim 28, wherein the latch circuit transmits a second latch signal to the charge pump when the pulse width modulated voltage is in a low state, wherein the second latch signal prevents the undershoot condition.

32. The regulator of claim 31, wherein the second latch signal prevents the output of the charge pump from decreasing further.

33. The regulator of claim 26, wherein the latch circuit comprises:

a first SR latch;

a second SR latch, wherein an input of the second SR latch comprises the pulse width modulated signal;

a first gate, wherein an input of the first gate comprises an output from the second SR latch and an input signal, wherein an output of the first gate comprises a first latch signal to

the charge pump, wherein the first latch signal prevents the overshoot condition; and

a second gate, wherein an input of the second gate comprises an output from the first SR latch and the input signal, wherein an output of the second gate comprises a second latch signal to the charge pump, wherein the second latch signal prevents the undershoot condition.

34. The regulator of claim 33, wherein the latch circuit further comprises:

a first D flip-flop coupled between the first SR latch and the second gate; and

a second D flip-flop coupled between the second SR latch and the first gate.

35. The regulator of claim 26, wherein the comparator circuit comprises:

a clock circuit; and

an inverter coupled to an output of the clock circuit.

36. The regulator of claim 26, wherein the comparator circuit comprises:

a clock circuit; and

a pulse generator coupled to an input of the clock circuit.